0300 #3

PATENT
Attorney Docket 83093

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: The application of	:	
James M. Seals et al	:	Group Art Unit:
	:	
Serial No.: 09/898,360	:	Examiner:
	:	
Filed: July 3, 2001	:	
	:	
For: Video Converter Board	:	

Assistant Commissioner for Patents
Box Non-Fee
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

The purpose of this Preliminary Amendment is to submit formal drawings and to modify the specification to conform to the formal drawings.

In the Drawings

Please replace the existing informal drawings (Figs. 1, 2 (2A and 2B), 3 (3A and 3B) and (4)) with the enclosed formal drawings (Figs. 1, 2 (2A, 2B and 2C), 3 (3A and 3B) and (4)).

In the Specification

Page 5, lines 19-21, please replace with the following paragraph:

Fig. 2 is composed of Figs. 2(A), 2(B) and 2(C) that cumulatively illustrate a block diagram of the video converter board of the present invention.

Page 6, lines 5-8, please replace with the following paragraph:

Fig. 4 illustrates the memory control sequences utilized for providing the refresh cycles generated by the video converter board of Fig. 2(B).

Page 6, line 11 through page 7 line 24, please replace with the following paragraph:

Referring to the drawings wherein the same reference number indicates the same element throughout, there is shown in Fig. 1 a block diagram, wherein the video converter board 10 of the present invention is interposed between a first subsystem 14 and a second system 16 and allows the first display system 14 to transfer signals to the second display system 16 which may be a remote monitor or flat panel. The display system 14 provides an output comprised of stroke/raster video data on signal path 18

which is actually comprised of three lines respectively carrying X deflection (X Def), Y deflection (Y Def), and Video signals, whereas the video converter board 10 converts the information embodied in the stroke/raster video on signal path 18 into a RGB video data format. More particularly, the video converter board 10 reformats the information carried by the raster/stroke transmission scheme into a RGB video data format responsive to a sync-on-green signal. Specifically, the video converter board 10 reformats its received information and provides output data in the RGB video data format so that it may be received and presented by the display system 16 requiring a serial interface on signal path 20 conforming to an Electronic Industry Association (EIA) standard, such as, a serial interface formatted in accordance with RS-343A standard. To our understanding, the RS-343A is the only standard that supports RGB video, but it is contemplated that the present invention will be applicable to other standards if such exist that support RGB video. In general, the display system 14 generates stroke/raster video only. The video converter board 10 converts the stroke/raster video into RGB so that the display subsystem 16 that uses RGB video will accept and display the video information generated by the display system 14. In one of

its embodiments, the video converter board 10 generates monochrome video only i.e., the video converter board 10 generates green video on a black background, wherein Red and Blue colors are not used. However, the video converter board 10 provides the functions to satisfy the requirements of the RGB format, sometimes referred to as SOG video. The operation of the video converter board 10 may be further described with reference to Fig. 2 composed of Figs. 2(A), 2(B), and 2(C).

Page 11, line 2 (of text) through page 12 line 2, replace with the following paragraph:

In general, and with simultaneous reference to Figs. 2(A), 2(B) and 2(C), the A/D front-end circuitry 22 receive the X deflection (XDEF), Y deflection (YDEF) signals, and the Video-In signals all of which are present on signal path 18. The analog-to-digital front-end circuitry 22 samples, at a predetermined rate, the X deflection, Y deflection and Video In signals and converts each sample signal into a corresponding digital quantity that is delivered to the memory 24 comprised of a plurality of banks 24J, 24K, and 24L. Memory control circuitry 26 sequentially selects each of the plurality of banks 24J, 24K, and 24L.

Page 12, lines 4-12, replace with the following paragraph:

The elements 24A, 24B, and 24C, shown in Fig. 2(B), serve as buffers that provide address information generated by A/D elements 22D and 22E and for writing to memory banks 24J, 24K, and 24L. The element 22F, shown in Fig. 2(A), is the A/D converter that serves the video-in data. The elements 24D, 24E, and 24F serve as buffers that provide video data info generated by A/D element 22F and are used for the actual video data written to memory banks 24J, 24K, and 24L, shown in Fig. 2(B). The elements 24G, 24H, and 24I serve as data buffers that provide blank data for memory blanking purposes to be described hereinafter.

Page 13, lines 1-5, replace with the following paragraph:

The converter D/A output circuitry 28, shown in Fig. 2(C), receives the RGB video formatted data from memory 24 and responds to the synchronization control circuitry 30, and generates the SOG signal along with the RGB video on signal path 20 and in a manner conforming to the serial interface requirements of the display system 16.

Page 13, lines 7-12, replace with the following paragraph:

The power subsystem 34 comprises a conventional DC to DC converter 34A that receives + 12 volt input from the VME Bus 34B. The VME Bus 34B also supplies the + 5 volt excitation for the digital circuitry shown in Fig. 2(C). The DC to DC converter generates the +5V and -5V excitation also used for the analog circuitry shown in Fig. 2.

Page 13, line 14 through page 14, line 2, replace with the following paragraph:

The timing and control subsystem 32, shown in Fig. 2(A), comprises the element 32A which generates 80 MHz clock that is routed to element 32B by way of signal path 38. The element 32B which is a clock driver delivers a 80 MHz clock that is supplied on signal path 40 to element 30A, as well as to the elements 24J, 24K, 24L, (see Fig. 2(B)), 30B, 30C, 30D, and 28 (see Fig. 2(C)). The element 32B of Fig. 2(A) also delivers the 80 MHz clock that is applied to element 26D by way of signal path 42. Element 26D divides the 80 MHz signal to 40 MHz and delivers such to element 32C. Element 32C is a clock driver that drives elements 22D, 22E, 22F, 22G, 22H, and 22I. The element 26D, in response to its received signal on signal path 42, generates the timing signals to elements 26A, 26B, and 26C, shown in Fig. 2(B), by way of signal path 46.

Page 14, lines 4-12, replace with the following paragraph:

The elements 22A, 22B, 22C, shown in Fig. 2(A), receive the XDEF, YDEF, and video-in signals on signal path 18 and each of these elements 22A, 22B, and 22C has the provisions for adjusting their gain and offset parameters respectively. The gain and offset parameters, known in the art, are used to adjust for slight variations in the stroke/raster video signals (XDEF, YDEF, and Video-in). The output of elements 22A, 22B, and 22C are respectively routed to elements 22D, 22E, and 22F each of which is an A/D converter operated at 40 MHz sampling rate.

Page 14, lines 14-22, replace with the following paragraph:

The elements 22D and 22E each provide a 10-bit digital quantity that are respectively routed to elements 22G and 22H, whereas element 22F provides an 8-bit digital quantity that is routed to element 22I. The output of elements 22G and 22H are combined together so as to provide a 20-bit quantity, serving as a memory address, that is respectively routed, via signal path 56, to elements 24A, 24B, and 24C, shown in Fig. 2(B), whereas element 22I provides a 8-bit quantity, serving as video data that is routed, via signal path 58 to elements 24D, 24E, and 24F, shown in Fig. 2(A).

Page 15, lines 1-5, replace with the following paragraph:

The elements 24A, 24B, and 24C, shown in Fig. 2(B), respectively route their 20-bit output information to inputs of elements 24J, 24K, and 24L, serving as selectable memory banks. Similarly, elements 24D, 24E, and 24F, shown in Fig. 2(A), respectively route their 8-bit quantity to the respective inputs of elements 24J, 24K, and 24L, shown in Fig. 2(B).

Page 15, lines 14-23, replace with the following paragraph:

The elements 24J, 24K, and 24L each serve as a memory bank each having a typical capacity of about 1 Mega (M) byte and are respectively selected by elements 26A, 26B, and 26C respectively by way of signal paths 66, 68, and 70 respectively. The memory banks 24J, 24K, and 24L, are responsive to the synchronization control circuit 26D and of elements 30C, 30D, and for read and blank addressing shown in Fig. 2(C). The element 26D, shown in Fig. 2(A), (memory control sequencer) controls the selection of the memory banks 24J, 24K and 24L, shown in Fig. 2(B), whereas elements 30C and 30D, shown in Fig. 2(C), provide addressing lines for reading and blanking purposes.

Page 16, lines 1-14, replace with the following paragraph:

The synchronization control circuit 30 has a first routine (to be described with reference to Fig. 3) of generating timing

for the sync-on-green (SOG) signal using elements 30A and 30B, shown in Fig. 2(C), and a second routine (to be described with reference to Fig. 3) for generating the memory addresses for reading and blanking the selected memory bank 24J, 24K, or 24L, shown in Fig. 2(B), using elements 30C and 30D, shown in Fig. 2(C). More particularly, elements 30A and 30B control the generation of the SOG signals and elements 30C and 30D control the memory addresses for reading and blanking. The synchronization control circuitry 30 generates the memory addresses to be read from the memory banks 24J, 24K, and 24L, shown in Fig. 2(B), on signal path 72 and the command for generating the blank data on the memory data bus on signal path 74, both of which paths are further shown in Figs. 2(B) and 2(C).

Page 16, lines 16-25, replace with the following paragraph:

The memory address reading path 72 of Fig. 2(C) is routed to elements 24M, 24N, and 24O of Fig. 2(B) which respectively, in turn, respond by supplying corresponding signals 76, 78, and 80, respectively carried three separate buses which, in turn, are routed to elements 24J, 24K, and 24L. Each of the elements, 24J, 24K, and 24L provides output signals which is representative of read data on signal path 82 representative of

video data which, in turn, is routed to the D/A output circuitry 28 shown on Fig. 2(C).

Page 19, lines 8-20, replace with the following paragraph:

At the end of producing 1024 lines, element 30B detects that the counter has counted to 1023 and generates the timing for the vertical sync pulse 94 shown in Fig. 3(B) having a typical duration of 18.8 ms (53.3(Hz)). Again, this signal is comprised of a front porch 88 and a back porch 90 portions. However, signal 94 includes a vert sync portion 96 instead of horiz sync portion 86. This signal 94 is typically quite longer than that of the horizontal pulses because the gun has to travel from the bottom of the screen to the top of the screen. These signals 84 and 94 also give reason to the name "sync-on-green". The data 92 and the sync pulses of signals 84 and 94 all travel on the green signal, thus there is only one output of the VCB 10 delivered by D/A output circuitry 28, shown in Fig. 2(C).

REMARKS

The transition from informal drawings to formal drawings necessitated changing the existing illustration of Fig. 2(A) into the enclosed illustrations of Fig. 2(A) and 2(B), which, in turn, necessitated the changes to the specification. The specification has been amended to allow the reader to more

easily locate the elements of Fig. 2 now spread between Figs. 2(A), 2(B) and 2(C) rather than the previous (informal drawings) confinement to Figs. 2(A) and 2(B).

The changes to the drawings and the specification did not add any new matter and the entrance of this Preliminary Amendment is respectfully requested.

Respectfully solicited,
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CERTIFICATE OF MAILING

I hereby certify that this paper (along with any referred to as being attached or enclosed is being deposited with the United States Postal Service on the date shown below with sufficient postage as to be sent by First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, DC 20231.

Date: September 25, 2001 Deborah A. Hughes

VERSION SHOWING CHANGES MADE

In the Drawings

Attached are informal drawings Figs. 2(A) and 2(B) marked in red, to generally outline the changes made to provide for the formal drawings.

In the Specification

Page 5, lines 19-21, has been amended as follows:

Fig. 2 is composed of Figs. 2(A), [and] 2(B), and 2(C) that cumulatively illustrate a block diagram of the video converter board of the present invention.

Page 6, lines 5-8, has been amended as follows:

Fig. 4 illustrates the memory control sequences utilized for providing the refresh cycles generated by the video converter board of Fig. [2A] 2(B).

Page 6, line 11, has been amended as follows:

Referring to the drawings wherein the same reference number indicates the same element throughout, there is shown in Fig. 1 a block diagram, wherein the video converter board 10 of the present invention is interposed between a first subsystem 14 and a second system 16 and allows the first display system 14 to

transfer signals to the second display system 16 which may be a remote monitor or flat panel. The display system 14 provides an output comprised of stroke/raster video data on signal path 18 which is actually comprised of three lines respectively carrying X deflection (X Def), Y deflection (Y Def), and Video signals, whereas the video converter board 10 converts the information embodied in the stroke/raster video on signal path 18 into a RGB video data format. More particularly, the video converter board 10 reformats the information carried by the raster/stroke transmission scheme into a RGB video data format responsive to a sync-on-green signal. Specifically, the video converter board 10 reformats its received information and provides output data in the RGB video data format so that it may be received and presented by the display system 16 requiring a serial interface on signal path 20 conforming to an Electronic Industry Association (EIA) standard, such as, a serial interface formatted in accordance with RS-343A standard. To our understanding, the RS-343A is the only standard that supports RGB video, but it is contemplated that the present invention will be applicable to other standards if such exist that support RGB video. In general, the display system 14 generates stroke/raster video only. The video converter board 10 converts the stroke/raster video into RGB so that the display subsystem 16 that uses RGB video will accept and display the video

information generated by the display system 14. In one of its embodiments, the video converter board 10 generates monochrome video only i.e., the video converter board 10 generates green video on a black background, wherein Red and Blue colors are not used. However, the video converter board 10 provides the functions to satisfy the requirements of the RGB format, sometimes referred to as SOG video. The operation of the video converter board 10 may be further described with reference to Fig. 2 composed of Figs. 2(A), 2(B), [and], ,and 2(C).

Page 11, line 2 (of text) through page 12 line 2, has been amended as follows:

In general, and with simultaneous reference to Figs. 2(A), 2(B) and 2(C), the A/D front-end circuitry 22 receive the X deflection (XDEF), Y deflection (YDEF) signals, and the Video-In signals all of which are present on signal path 18. The analog-to-digital front-end circuitry 22 samples, at a predetermined rate, the X deflection, Y deflection and Video In signals and converts each sample signal into a corresponding digital quantity that is delivered to the memory 24 comprised of a plurality of banks 24J, 24K, and 24L. Memory control circuitry 26 sequentially selects each of the plurality of banks 24J, 24K, and 24L.

Page 12, lines 4-12, has been amended as follows:

The elements 24A, 24B, and 24C, shown in Fig. 2(B), serve as buffers that provide address information generated by A/D elements 22D and 22E and for writing to memory banks 24J, 24K, and 24L. The element 22F, shown in Fig. 2(A), is the A/D converter that serves the video-in data. The elements 24D, 24E, and 24F serve as buffers that provide video data info generated by A/D element 22F and are used for the actual video data written to memory banks 24J, 24K, and 24L, shown in Fig. 2(C). The elements 24G, 24H, and 24I serve as data buffers that provide blank data for memory blanking purposes to be described hereinafter.

Page 13, lines 1-5, has been amended as follows:

The converter D/A output circuitry 28, shown in Fig. 2(C), receives the RGB video formatted data from memory 24 and responds to the synchronization control circuitry 30, and generates the SOG signal along with the RGB video on signal path 20 and in a manner conforming to the serial interface requirements of the display system 16.

Page 13, lines 7-12, has been amended as follows:

The power subsystem 34 comprises a conventional DC to DC converter 34A that receives + 12 volt input from the VME Bus 34B. The VME Bus 34B also supplies the + 5 volt excitation for

the digital circuitry shown in Fig. [2] 2(C). The DC to DC converter generates the +5V and -5V excitation also used for the analog circuitry shown in Fig. 2.

Page 13, line 14, page 14, line 2, has been amended as follows:

The timing and control subsystem 32, shown in Fig. 2(A), comprises the element 32A which generates 80 MHz clock that is routed to element 32B by way of signal path 38. The element 32B which is a clock driver delivers a 80 MHz clock that is supplied on signal path 40 to element 30A, as well as to the elements 24J, 24K, 24L, (see Fig. 2(B)), 30B, 30C, 30D, and 28 (see Fig. 2(C)). The element 32B of Fig. 2(A) also delivers the 80 MHz clock that is applied to element 26D by way of signal path 42. Element 26D divides the 80 MHz signal to 40 MHz and delivers such to element 32C. Element 32C is a clock driver that drives elements 22D, 22E, 22F, 22G, 22H, and 22I. The element 26D, in response to its received signal on signal path 42, generates the timing signals to elements 26A, 26B, and 26C, shown in Fig. 2(B), by way of signal path 46.

Page 14, lines 4-12, has been amended as follows:

The elements 22A, 22B, 22C, shown in Fig. 2(A), receive the XDEF, YDEF, and video-in signals on signal path 18 and each of

these elements 22A, 22B, and 22C has the provisions for adjusting their gain and offset parameters respectively. The gain and offset parameters, known in the art, are used to adjust for slight variations in the stroke/raster video signals (XDEF, YDEF, and Video-in). The output of elements 22A, 22B, and 22C are respectively routed to elements 22D, 22E, and 22F each of which is an A/D converter operated at 40 MHz sampling rate.

Page 14, lines 14-22, has been amended as follows:

The elements 22D and 22E each provide a 10-bit digital quantity that are respectively routed to elements 22G and 22H, whereas element 22F provides an 8-bit digital quantity that is routed to element 22I. The output of elements 22G and 22H are combined together so as to provide a 20-bit quantity, serving as a memory address, that is respectively routed, via signal path 56, to elements 24A, 24B, and 24C, shown in Fig. 2(B), whereas element 22I provides a 8-bit quantity, serving as video data that is routed, via signal path 58 to elements 24D, 24E, and 24F, shown in Fig. 2(A).

Page 15, lines 1-5, has been amended as follows:

The elements 24A, 24B, and 24C, shown in Fig. 2(B), respectively route their 20-bit output information to inputs of elements 24J, 24K, and 24L, serving as selectable memory banks.

Similarly, elements 24D, 24E, and 24F, shown in Fig. 2(A), respectively route their 8-bit quantity to the respective inputs of elements 24J, 24K, and 24L, shown in Fig. 2(B).

Page 15, lines 14-23, has been amended as follows:

The elements 24J, 24K, and 24L each serve as a memory bank each having a typical capacity of about 1 Mega (M) byte and are respectively selected by elements 26A, 26B, and 26C respectively by way of signal paths 66, 68, and 70 respectively. The memory banks 24J, 24K, and 24L, are responsive to the synchronization control circuit 26D and of elements 30C, 30D, and for read and blank addressing shown in Fig. 2 [(B)](C). The element 26D, shown in Fig. 2(A), (memory control sequencer) controls the selection of the memory banks 24J, 24K and 24L, shown in Fig. 2(B), whereas elements 30C and 30D, shown in Fig. 2(C), provide addressing lines for reading and blanking purposes.

Page 16, lines 1-14, has been amended as follows:

The synchronization control circuit 30 has a first routine (to be described with reference to Fig. 3) of generating timing for the sync-on-green (SOG) signal using elements 30A and 30B, shown in Fig. 2(C), and a second routine (to be described with reference to Fig. 3) for generating the memory addresses for reading and blanking the selected memory bank 24J, 24K, or 24L,

shown in Fig. 2(B), using elements 30C and 30D, shown in Fig. 2(C). More particularly, elements 30A and 30B control the generation of the SOG signals and elements 30C and 30D control the memory addresses for reading and blanking. The synchronization control circuitry 30 generates the memory addresses to be read from the memory banks 24J, 24K, and 24L, shown in Fig. 2(B), on signal path 72 and the command for generating the blank data on the memory data bus on signal path 74, both of which paths are further shown in Figs. 2[(A)](B) and 2[(B)](C).

Page 16, lines 16-25, has been amended as follows:

The memory address reading path 72 of Fig. 2 [(B)](C) is routed to elements 24M, 24N, and 24O of Fig. 2 [(A)](B) which respectively, in turn, respond by supplying corresponding signals 76, 78, and 80, respectively carried three separate buses which, in turn, are routed to elements 24J, 24K, and 24L. Each of the elements, 24J, 24K, and 24L provides output signals which is representative of read data on signal path 82 representative of video data which, in turn, is routed to the D/A output circuitry 28 shown on Fig. 2 [(B)](C).

Page 19, lines 8-20, has been amended as follows:

At the end of producing 1024 lines, element 30B detects that the counter has counted to 1023 and generates the timing for the vertical sync pulse 94 shown in Fig. 3(B) having a typical duration of 18.8 ms (53.3(Hz)). Again, this signal is comprised of a front porch 88 and a back porch 90 portions. However, signal 94 includes a vert sync portion 96 instead of horiz sync portion 86. This signal 94 is typically quite longer than that of the horizontal pulses because the gun has to travel from the bottom of the screen to the top of the screen. These signals 84 and 94 also give reason to the name "sync-on-green". The data 92 and the sync pulses of signals 84 and 94 all travel on the green signal, thus there is only one output of the VCB 10 delivered by D/A output circuitry 28, shown in Fig. 2(C).

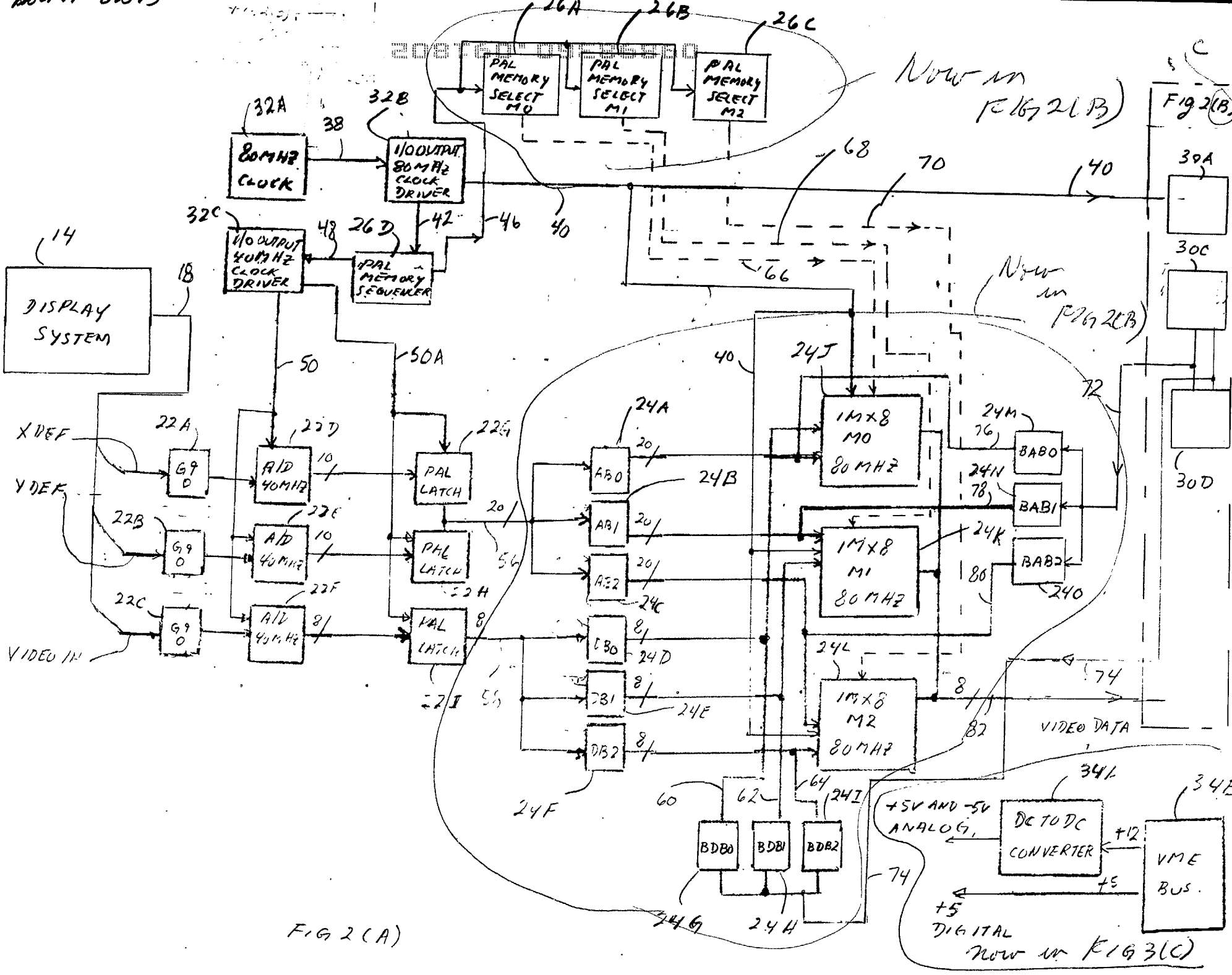
PAL MEMORY SELECT M0
PAL MEMORY SELECT M1
PAL MEMORY SELECT M2
80MHz CLOCK
I/O OUTPUT 80 MHz CLOCK DRIVER
I/O OUTPUT 40 MHz CLOCK DRIVER
PAL MEMORY SEQUENCER
DISPLAY SYSTEM
XDEF
YDEF
VIDEO IN
G9 D
G9 O
A/D 40MHz
PAL LATCH
1M x 8 M0 80 MHz
1M x 8 M1 80 MHz
1M x 8 M2 80 MHz
BABO
BABI
BAB2
ABO
AB1
AB2
DBO
DB1
DB2
BDBO
BDB1
BDB2
VIDEO DATA
DC TO DC CONVERTER
+5V AND -5V ANALOG
+12
+5
+5 DIGITAL
VME BUS
Now in FIG 2(B)
Now in FIG 2(B)
Now in FIG 3(C)

FIG 2(A)

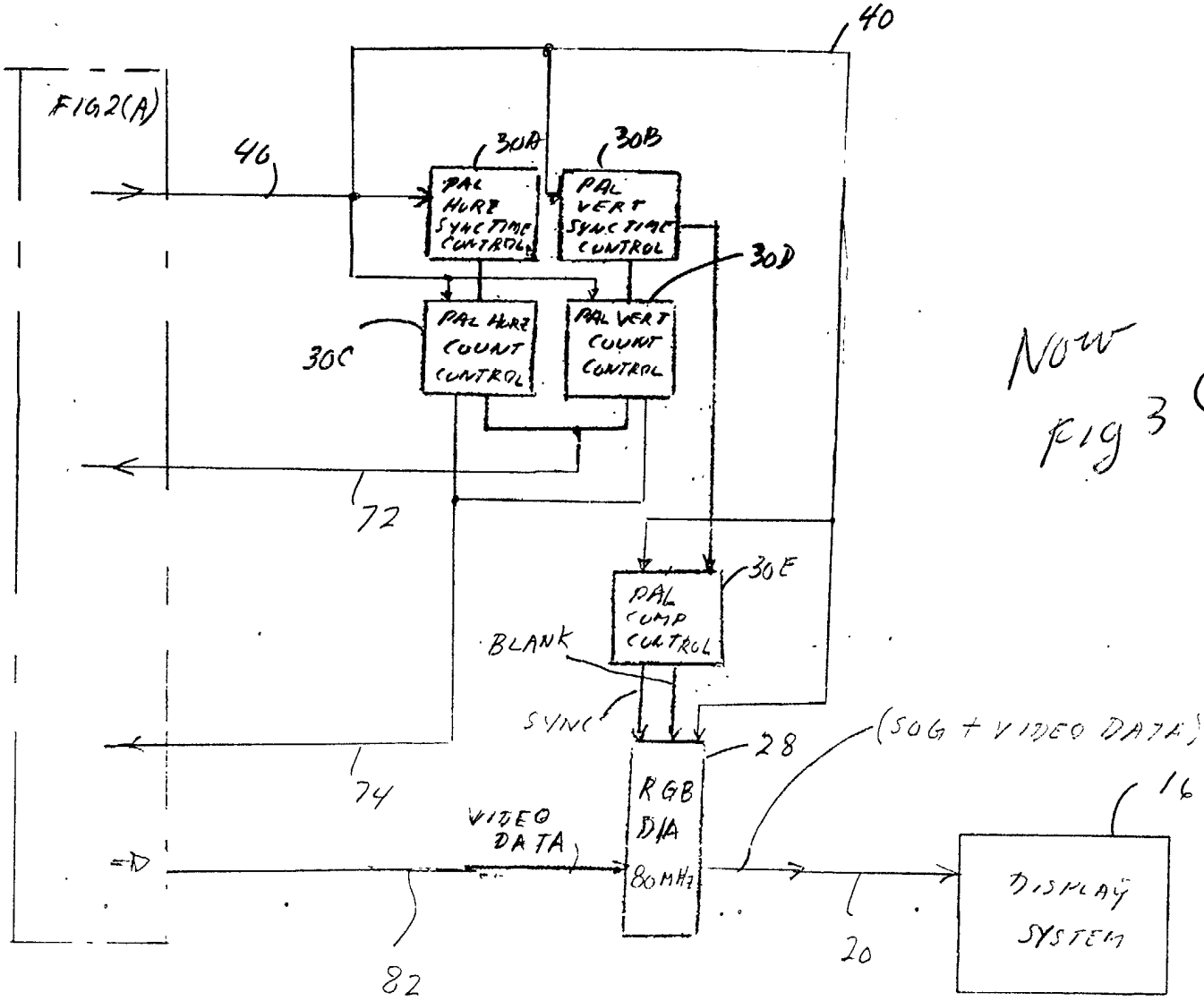

FIG2(B)

Now Fig 3(C)